REMARKS

Claims 1-13 and 17-22 are pending. Claims 1, 3, 7-11, 13, 17, 18, and 21 have been amended for clarity.

1. Rejections based on Spivey et al. in view of Heller et al.:

Claims 1, 2, 5-7, 9-13, and 17-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,886,353 to Spivey et al. in view of U.S. Pat. No. 6,396,539 to Heller et al. Applicants respectfully traverse this rejection.

Claim 1 has been amended to clarify that the CMOS image sensor circuit includes "a CMOS image sensor chip comprising an image sensor portion comprising an array of pixels arranged in rows and columns," and "a control portion comprising image sensor logic, said image sensor logic being electrically connected to said image sensor portion." The image sensor logic includes "row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually, said image sensor portion having a first area and a second area." The chip is formed to have at least "a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." Claim 1 has been further clarified to recite that the image sensor portion includes "imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said substrate and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said substrate." The row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion," and "a pixel interpolator and said chip driver circuitry

located between said first area and said second area of said image sensor portion and said fourth edge of said substrate."

Spivey et al. discloses an imager chip having row shift registers 186 formed on one edge of imager array 190, as shown in Fig. 17A. The Office Action attempts to meet the present invention recited in claim 1 by combining two of the imager chips disclosed in the reference to Spivey et al. The combined imager chips of Spivey et al. do not provide "a CMOS image sensor chip comprising an image sensor portion comprising an array of pixels arranged in rows and columns formed on said chip," and "a control portion comprising image sensor logic formed on said chip, said image sensor logic being electrically connected to said image sensor portion." Instead, combining two imager chips of Spivey et al. provides two CMOS imager chips including two image sensor portions, one on each chip, and two control portions, one on each chip, connected respectively to each of the two image sensor portions.

Further, combining two of the imager chips disclosed in Spivey et al. does not produce an imager chip having "a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge" so as to have "imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said substrate and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said substrate." Instead, the two imager chips of Spivey et al. have two arrays 190, each with its own row shift register 186. More specifically, the first array 190 extends on the first imager chip from the first edge to the row shift register 186, which is along the second edge of the first imager chip, next to the abutting imager chip. The

second array 190 extends over the second imager chip from the first edge to the row shift register 186 along the second edge of the second imager chip.

Fundamentally, two of the chips disclosed by Spivey et al. do not combine to produce "an imager chip." Even if one properly could ignore the edge between the two imager chips of Spivey et al., as would be required to obtain "an imager chip" from the combination proposed in the Office Action, the imager arrays 190 do not extend between first and second parallel edges, but rather extend from the first edge to the row shift register 186. Moreover, Spivey et al. also does not teach or suggest that the row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." Applicant respectfully submits that the interpretation of the Spivey et al. reference proposed in the Office Action requires a strained reading of the reference, the awkwardness of which is indicative of an improper hindsight attempt to shoehorn the disclosure of Spivey et al. into the invention of claim 1.

Heller et al. does not cure the deficiencies of Spivey et al. Heller et al. has been cited as providing on-chip interpolation circuitry. Heller et al. discloses an image sensor having an array 12 and readout circuitry located separately on a substrate 10. Heller et al. does not supply the necessary motivation to modify Spivey et al. in the manner suggested by the Examiner. Claim 1 and its dependent claims 2-7 and 19-21 are patentable over Spivey et al. in view of Heller et al.

Claim 9 has been amended to clarify that a CMOS imager includes "a first CMOS image sensor chip having an image sensor portion arranged in an array of rows and columns" with "a control portion and a centralized row-local control portion." The centralized row-local control portion is "physically located inside the image sensor portion in place of a plurality of pixels of the array forming the CMOS image sensor

portion." The centralized row-local control portion thereby forms "at least two image sensor areas, said control portion including a pixel interpolator located between said at least two image sensor areas and one of said edges of said first CMOS image sensor chip."

As noted above, Spivey et al. and Heller et al. even considered together do not teach or suggest "a first CMOS image sensor chip having a control portion and a centralized row-local control portion." More specifically, the "centralized row-local control portion" is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said CMOS image sensor portion." The centralized row-local portion forms "at least two image sensor areas." Claim 9 and its dependent claims 10-22 are patentable over the cited references to Spivey et al. and Heller et al.

Claim 11 recites a method of fabricating a CMOS imager by "fabricating at least two CMOS image sensor chips having an image sensor portion arranged in an array of rows and columns," and having "a control portion and a centralized row-local control portion, said centralized row-local control portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming formed on said image sensor chip." The centralized row-local control portion thereby forms "at least two image sensor areas for each of said at least two CMOS image sensor chips." The at least two CMOS image sensor chips are butted together, and the "control portions of said at least two CMOS image sensor chips" are integrated "such that said at least two CMOS image sensors chips function as a single CMOS imager."

Spivey et al. and Heller et al. do not, even when considered together, teach or suggest a method of fabricating a CMOS imager made of two CMOS imager chips, each chip having "a centralized row-local control portion, said centralized row-local control

portion being physically located inside said image sensor portion in place of a plurality of pixels of the array forming formed on said image sensor chip." Further, Spivey et al. and Heller et al. not teach or suggest a method of making a CMOS imager in which the centralized row-local control portion forms "at least two image sensor areas." Claim 11 and its dependent claim 12 are patentable over the cited references to Spivey et al. and Heller et al.

Claim 13 recites a CMOS image sensor circuit that includes "a first CMOS image sensor chip having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said chip substrate." The image sensor logic is "electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than said rows individually." The image sensor portion has "a first area and a second area." The first CMOS image sensor chip is "formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, said second set of parallel edges including a third edge and a fourth edge." The first CMOS image sensor portion extends "between said first edge, said second edge, and said third edge, such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor chip substrate and said second area of said image sensor portion is adjacent said second edge and said third edge of said first CMOS image sensor chip substrate." The row logic is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." A pixel interpolator and the chip driver circuitry is "located between said first portion and said second portion of said image sensor portion and said fourth edge of said image sensor chip substrate. The image sensor circuit has "a second CMOS image sensor chip configured similarly to said first

CMOS image sensor chip and abutted to one of said edges of said first CMOS image sensor chip."

Spivey et al. and Heller et al. do not, even when considered together, teach or suggest an image sensor with a first CMOS image sensor portion with first and second areas that extends between a first edge, a second edge, and a third edge, "such that said first area of said image sensor portion is adjacent said first edge and said third edge of said image sensor chip substrate and said second area of said image sensor portion is adjacent said second edge and said third edge of said first CMOS image sensor chip." Further, the proposed combination does not produce row logic that is "physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." Consequently, Spivey et al. and Heller et al. do not combine to produce an image sensor circuit that has "a second CMOS image sensor chip configured similarly to said first CMOS image sensor chip and abutted to one of said edges of said first CMOS image sensor chip." Claim 13 is patentable over Spivey et al. in view of Heller et al.

Claim 17 recites a method of fabricating a CMOS imager including "fabricating at least two CMOS image sensor chips having an image sensor portion arranged in an array of rows and columns," wherein each of the image sensor chips has "a control portion and a centralized row-local control portion." The centralized row-local control portion is "physically located inside said image sensor portion in place of a plurality of pixels of the array formed on said image sensor chip." The arrangement thereby forms "at least two active image sensor areas in each of said at least two CMOS image sensor chips."

Spivey et al. and Heller et al. do not, even when considered together, teach or suggest a method of making image sensor chips having a row-control portion located

along one edge of the chip. Spivey et al. does not teach or suggest manufacturing an image sensor made up of image sensor chips having "a centralized row-local control portion" that is "physically located inside said image sensor portion in place of a plurality of pixels of the array formed on said image sensor chip." Claim 17 is patentable over Spivey et al. in view of Heller et al. Claim 18 is dependent on claim 17, and is patentable for at least the same reasons.

2. Rejection of claims 3, 4, and 8 over Spivey et al. in view of Heller et al. and Spartiotis et al.:

Claims 3, 4, and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Spivey et al. in view of Heller et al. in further view of U.S. Appl. Pub. No. 2002/000549 to Spartiotis et al. Applicants respectfully traverse this rejection.

Claims 3 and 4 depend from claim 1, and are patentable for at least the reasons set forth above. Spartiotis et al. does not cure the deficiencies of Spivey et al. and Heller et al. Spartiotis et al. discloses that imager chips are cut with diamond saws to a precision of 10-20 microns. Spartiotis et al. does not combine with Spivey et al. and Heller et al. to teach or suggest "a CMOS image sensor chip comprising an image sensor portion comprising an array of pixels arranged in rows and columns formed on said chip" and having "a control portion comprising image sensor logic formed on said chip, said image sensor logic being electrically connected to said image sensor portion." Spartiotis et al. also does not combine with Spivey et al. and Heller et al. to produce a CMOS image sensor circuit with "imaging pixels extending between said first edge, said second edge, and said third edge, such that imaging pixels of said first area of said image sensor portion are adjacent said first edge and said third edge of said substrate and imaging pixels of said second area of said image sensor portion are adjacent said second edge and said third edge of said substrate." In addition, Spartiotis et al. does not combine with Spivey et al. and Heller et al. to teach or suggest that the row logic is

"physically located inside said image sensor portion in place of a plurality of pixels of the array forming said image sensor portion." Claims 3 and 4 are patentable over the Spivey et al. in view of Heller et al. in further view of Spartiotis et al.

Claim 8 recites a method of capturing an image by "providing at least two image sensor chips, each chip having first and second edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges." Each image sensor chip "includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array." The method further includes "abutting said image sensor chips along at least one of corresponding first and second edges," and "interpolating missing pixels on said chips, the missing pixels being caused by both said row select logic and by spaces between pixel pitches along abutted edges of said image sensor chips."

Spivey et al., Heller et al., and Spartiotis et al. do not, even when considered together, teach or suggest "at least two image sensor chips, each chip having first and second edges and an image sensor array of imaging pixels that comes within two pixel pitches of said first and second edges, and includes a control portion with row selecting logic in place of a plurality of central pixels of the image sensor array." The cited references do not teach or suggest a method of capturing an image by "abutting said image sensor chips along at least one of corresponding first and second edges." Claim 8 is patentable over Spivey et al. in view of Heller et al. in further view of Spartiotis et al.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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